Event System Troubleshooting Techniques

What is the Event System?

- Distribute Timing Signals
- Event Generators and Event Receivers
- What is an “Event”?
  - The occurrence of a unique timing signal
  - Code transmitted from an Event Generator
  - Received by Event Receivers
  - Currently have about 45 unique Events
  - Capacity of 255 Events
  - Multiple Event Generators

Why do we have Events?

- Used to generate timing signals
  - Can generate a VME Interrupt
    - Used to process records in IOC
  - Can generate a hardware timing signal
- Can increment time stamp counter
  - Synchronous throughout APS

Events

Ev #	Description	Source	Input
1	Linac PreTrigger	Inj EG 1	Trigger 0
2	Linac Trigger	Inj EG 1	Trigger 1
4	2 Hz	Inj EG 1	Trigger 3
47	SR Inject Trigger	Inj EG 2	Trigger 4
122	Heartbeat	Inj EG 2	VME

Hardware

EVG100 Event Generator

- Data Receive
  - Upstream EVG100
- Data Transmit
  - Downstream Event Generator
  - Local EVR100
- Out
  - PECL Fan Out
- LED's
  - Error
  - Data Transmit
  - Module Select
  - 10 MHz Clock

Hardware

EVR100 Event Receiver

- Receive
- Transmit
  - Repeater for daisy chain
- Clock Outputs
  - Synchronous
- LED's
  - Error
  - Data Received
  - Module Select
  - Interrupt

Hardware

EGI100 Event Generator Interface

- Eight Event Trigger inputs
- Two Event Sequence Trigger inputs
- Two Event Clock inputs
- Two External Sequence Reset inputs

Hardware

ERI100

Event Receiver Interface

- 32 Outputs
  - 4 Digital Delay Gen Pulses
  - 8 Trigger Event Outputs
  - 14 Pulse Outputs
  - 7 Level Outputs
- Plugs into rear, connects via P2

Interconnect

- Fiber optic link connects Event Generators to Event Receivers
- Fiber FanOut modules in Control Rooms
  - FOM106 PECL to 6 Fibers
- Fiber link uses standard multimode fiber with ST connectors
- FanOut chassis used in Linac
- RF area has additional Event Generators

What's on the fiber Link?

- Link uses TAXI chips – AMD 100Mbit protocol
- Sync signals always present
- Data (Event) sent at 10MHz rate
- Data is a number between 0 and 255

Event Generator

- Event Generator Events are caused by
  - Software
  - Input from upstream Event Generator
  - Input from EGI100 Event Generator Interface
    - Eight Event trigger inputs
    - Two Event Sequence trigger inputs
    - Two Event Clock inputs
    - Two External Event Sequence Reset inputs

Event Receiver

- Event is decoded
  - Address to mapping RAM
- Interrupts
  - Event
  - HeartBeat
- Timing signals
- Time Stamp
- Event must be enabled

Troubleshooting

- All Events generated in injtime are expected at all Event Receivers
  - Heartbeat
- If Event is enabled by software then
  - Timing Signal
  - Record processing

Check Event Receiver Led's

- Error LED
  - Checks Link Status
    - Bad Transmitter, Receiver or fiber
- Data Received
  - Checks for any Events
- Module Select
  - Indicates VME access
- Interrupt

ESD100 Event Detector (Event Snooper)

- Data Detect LED
- Event Detect LED
  - Selected Event present
  - Normal or Latch mode
- Violation LED
  - Bad Link
- Event Number switch
  - Input HEX
- Sync Output

Snooper Connection

- Fiber Input connects to Transmit Out of Event Receiver
- Could be connected to the input fiber link
- Test Heartbeat Event 122
  - Enter 7A on Snooper. Always enter HEX!

All Timing Signals missing from single location

- Most likely failure mode
  - Events not received due to bad fiber link
    - Problem with Fan Out module
      - Weak or bad transmitter
    - Problem with fiber jumper
  - Bad Event Receiver
  - IOC problem

Specific Timing signal missing from single location

- Event received and not decoded
  - Event Receiver
  - Event Receiver Interface or cables

Specific Timing signal missing from all locations

- Problem with Event Generator
  - Identify specific Event Generator
  - Inputs to Event Generator Interface
  - IOC problem

All Timing signals missing from all locations

- Event Generator
- Fan Out module

What if the Event is not present?

- Check Event at another location to be sure it's not a global problem
  - which would indicate problem in Control room timing racks
- Check fiber link all the way back to source using the Snooper
- Could I just look for light on the fiber?
  - Never a good idea to look at light on fiber optics- transmitter failure modes could be dangerous plus it's a bad habit.

Check Event Generator Led's

- Error LED
  - Checks up Link Status
    - Bad Transmitter, Receiver or fiber
- Data Transmit
  - Checks for any Events out
- Module Select
  - Indicates VME access
- Ignore 10MHz clock LED

Events_1

Timing System Events					
Event #	Hex	Description	Source EG	EG Input	Note
1	1	Linac PreTrigger	Inj EG #1	Trigger 0	
2	2	Linac Trigger	Inj EG #1	Trigger 1	
3	3	Last Bunch	Inj EG #1	Trigger 2	
4	4	2 Hz	Inj EG #1	Trigger 3	
5	5	60 Hz	Inj EG #1	Trigger 4	
9	9	Par Compress On	Inj EG # 2	Trigger 0	
10	A	Par Compress Off	Inj EG # 2	Trigger 1	
17	11	PAR BPM Start Scan	Inj EG # 2	Sequence Ram 1	
18	12	Loss Monitor Reset Set	Inj EG # 2	Sequence Ram 1	
19	13	Loss Monitor Reset Reset	Inj EG # 2	Sequence Ram 1	
20	14	Par Pulse Magnet Level Set	Inj EG # 2	Sequence Ram 1	
21	15	Par Pulsed Magnet Level Reset	Inj EG # 2	Sequence Ram 1	
22	16	RF cycle PreTrigger	Inj EG # 2	Sequence Ram 1	
23	17	Linac Start Burst Set	VME		
24	18	Linac Start Burst Reset	VME		
25	19	Linac PreTrigger Gate	Inj EG #2	Trigger 2	
26	1A	PSCU Sample Power Supply	Inj EG #2	Trigger 6	
27	1B				
28	1C				
29	1D	Par EKicker Charge On	Inj EG #2	Sequence Ram 1	
30	1E	Par EKicker Charge Off	Inj EG #2	Sequence Ram 1	
31	1F				
32	20				
33	21	Booster I PSCU C harge	Inj EG #2	Sequence Ram 1	
34	22	End of Last Bunch Seqeunce	Inj EG #2	Sequence Ram 1	set to 83 ms
35	23	Booster Inject PSCU Sample	Inj EG #2	Trigger 3	
36	24	Booster Start Ramp	Inj EG #1	Trigger 5	
37	25	Sample Par 12th Harmonic	Inj EG #2	Sequence Ram 1	Set to 60ms after compress on
38	26	Booster Start Ramp 2 RF	Inj EG #2	Sequence Ram 1	Set to 600 usec before Booster Start Ramp
39	27	Reset Par BPM timing Card	Inj EG #2	Sequence Ram 1	set to 80 ms
40	28	End of Booster Ramp Seq	Inj Eg #1	Sequence Ram 1	set to 250 ms
41	29	Booster Loss Monitor Reset On	VME		
42	2A	PAR 12th Harmonic VXI Trigger	Inj EG#2	Sequence Ram 1	60 ms after PAR compress On
43	2B	Booster 1Hz On	VME		
44	2C	Booster 1Hz Off	VME		
45	2D	SR Inject Triger	Mt Eg #1	Trigger 7	
46	2E	BS Inject Trigger	Inj EG #1	Trigger 6	
47	2F	SR Inject Trigger (ICR)	Inj EG #2	Trigger 4	

Events _2

48	30	SR Orbit Feedback Clock	Mt EG#2	Trigger 0	
49	31	SR Inject On			
50	32	SR Inject Off			
51	33	MPS Trip	Mt EG#1	Trigger 0	
52	34	TopUp Data Inhibit On	Mt EG#2	Trigger 2	
53	35	TopUp Data Inhibit Off	Mt EG#2	Trigger 3	
54	36	Linac Modulator Trigger	It EG#1	Trigger 7	
100	64	Used By RF EG			
101	65	Used By RF EG			
102	66	Used By RF EG			
103	67	Used By RF EG			
122	7A	HeartBeat	VME It		1 second period
123	7B	Reset Event Receiver PreScalers			
124	7C	1 kHz clock	Inj Eg #2	Trigger 0	
125	7D	Reset TimeStamp Counters	VME Mt		10 second period
126	7E	Freeze Event Sequence			Internal to EG
127	7F	End Event Sequence			Internal to EG

Just where is “the source”?

- Upstream
- Documentation
  - Wiring List on Web (Controls Timing Hardware)
  - ESD100 on Web
  - /asdctls/documentation/
  - CVCCT tool was used to generate a .pdf
    - /asdctls/documentation/online_systems/timing/event_link_cabling.pdf

F3

CRATE

Wiring List

A	B	C	D	E	F	G	H	I	J	K	L	M	N	O
C-000590-2		CC18		S_521_ETIM_O	VME#3	8	FOM103	FO Out4	iocs21bpm				A30	
C-000590-1		CC17		S_521_Event_O	VME#1	18	FOM106	FO Out4	iocs21bpm	5	EVR100	FO In	A29	
C-000590-6		CC22		S_521_Inhibit_O	VME#4	8	FOM100	Out 4	iocs21bpm	20	TIM101	FO In 0	A34	
C-000590-5		CC21		S_521_Init_O	VME#4	3	FOM100	Out 4	iocs21bpm	18	TIM100	FO In 0	A33	
C-000590-3		CC19		S_521_P0_O	VME#3	3	FOM103	FO Out 4	iocs21bpm	9	FOM117B	FO In A	A31	
C-000592-5		CC36		S_523_44MHz_O	VME#3	14	FOM106	Out 5	iocs23bpm	9	FOM117B	FO In B	A32	
C-000592-2		CC34		S_523_ETIM_O	VME#3	8	FOM103	FO Out5	iocs23bpm				A30	
C-000592-1		CC33		S_523_Event_O	VME#1	18	FOM106	FO Out5	iocs23bpm	5	EVR100	FO In	A29	
C-000592-7		CC38		S_523_Inhibit_O	VME#4	8	FOM100	Out 5	iocs23bpm	20	TIM101	In	A34	
C-000592-6		CC37		S_523_Init_O	VME#4	3	FOM100	Out 5	iocs23bpm	18	TIM100	FO In 0	A33	
C-000592-3		CC35		S_523_P0_O	VME#3	3	FOM103	FO Out 5	iocs23bpm	9	FOM117B	FO In A	A31	
C-000594-5		CC53		S_525_44MHz_O	VME#3	15	FOM106	Out 0	iocs25bpm	10	FOM117B	FO In B	A33	
C-000594-2		CC50		S_525_ETIM_O	VME#3	9	FOM103	FO Out0	iocs25bpm				A30	
C-000594-1		CC49		S_525_Event_O	VME#1	17	FOM106	FO Out0	iocs25bpm	5	EVR100	FO In	A29	
C-000594-7		CC55		S_525_Inhibit_O	VME#4	9	FOM100	Out 0	iocs25bpm	20	TIM101	In	A35	
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C-000594-3		CC51		S_525_P0_O	VME#3	4	FOM103	FO Out0	iocs25bpm	10	FOM117B	FO In A	A31	
C-000594-4		CC52		S_525_videoSync_O	VME#1	12	FOM103	FO Out3	iocs25bpm	20	TIM101	FO In 0	A32	
C-000596-4		CC68		S_527_44MHz_O	VME#3	15	FOM106	Out 1	iocs27bpm	12	FOM117B	FO In B	A32	
C-000596-2		CC66		S_527_ETIM_O	VME#3	9	FOM103	FO Out1	iocs27bpm				A30	
C-000596-1		CC65		S_527_Event_O	VME#1	17	FOM106	FO Out1	iocs27bpm	5	EVR100	FO In	A29	
C-000596-6		CC70		S_527_Inhibit_O	VME#4	9	FOM100	Out 1	iocs27bpm	20	TIM101	In	A34	
C-000596-5		CC69		S_527_Init_O	VME#4	4	FOM100	Out 1	iocs27bpm	18	TIM100	In 0	A33	
C-000596-3		CC67		S_527_P0_O	VME#3	4	FOM103	FO Out1	iocs27bpm	12	FOM117B	FO In A	A31	
C-000598-5		DD13		S_529_44MHz_O	VME#3	15	FOM106	Out 2	iocs29bpm	9	FOM117B	FO In B	A33	
C-000598-2		DD10		S_529_ETIM_O	VME#3	9	FOM103	FO Out2	iocs29bpm				A30	
C-000598-1		DD09		S_529_Event_O	VME#1	17	FOM106	FO Out2	iocs29bpm	5	EVR100	FO In	A29	
C-000598-7		DD15		S_529_Inhibit_O	VME#4	9	FOM100	Out 2	iocs29bpm	20	TIM101	FO In 0	A35	
C-000598-6		DD14		S_529_Init_O	VME#4	4	FOM100	Out 2	iocs29bpm	18	TIM100	FO In 0	A34	
C-000598-4		DD12		S_529_P0_O	VME#3	4	FOM103	FO Out 2	iocs29bpm	9	FOM117B	FO In A	A32	
C-000600-4		DD28		S_531_44MHz_O	VME#3	15	FOM106	Out 3	iocs31bpm	9	FOM117B	FO In B	A32	
C-000600-2		DD26		S_531_ETIM_O	VME#3	9	FOM103	FO Out3	iocs31bpm				A30	
C-000600-1		DD25		S_531_Event_O	VME#1	17	FOM106	FO Out3	iocs31bpm	5	EVR100	FO In	A29	
C-000600-6		DD30		S_531_Inhibit_O	VME#4	9	FOM100	Out 3	iocs31bpm	20	TIM101	FO In 0	A34	
C-000600-5		DD29		S_531_Init_O	VME#4	4	FOM100	Out 3	iocs31bpm	18	TIM100	FO In 0	A33	
C-000600-3		DD27		S_531_P0_O	VME#3	4	FOM103	FO Out 3	iocs31bpm	9	FOM117B	FO In A	A31	
C-000602-5		DD45		S_533_44MHz_O	VME#3	15	FOM106	Out 4	iocs33bpm	9	FOM117B	FO In B	A41	
C-000602-2		DD42		S_533_ETIM_O	VME#3	9	FOM103	FO Out4	iocs33bpm				A38	
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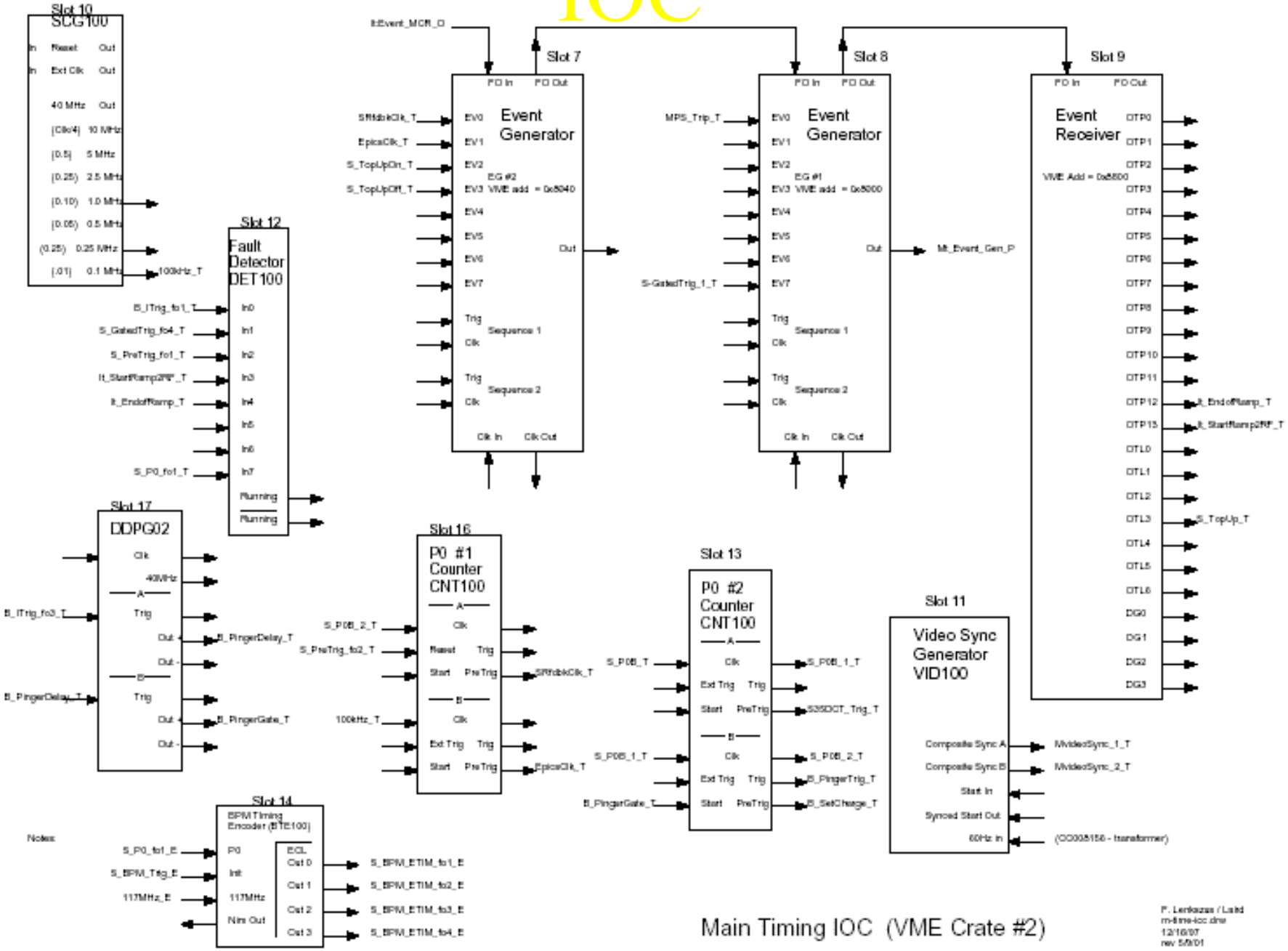
IOC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SCG100
In Reset Out
In Ext Clk Out
40 MHz Out
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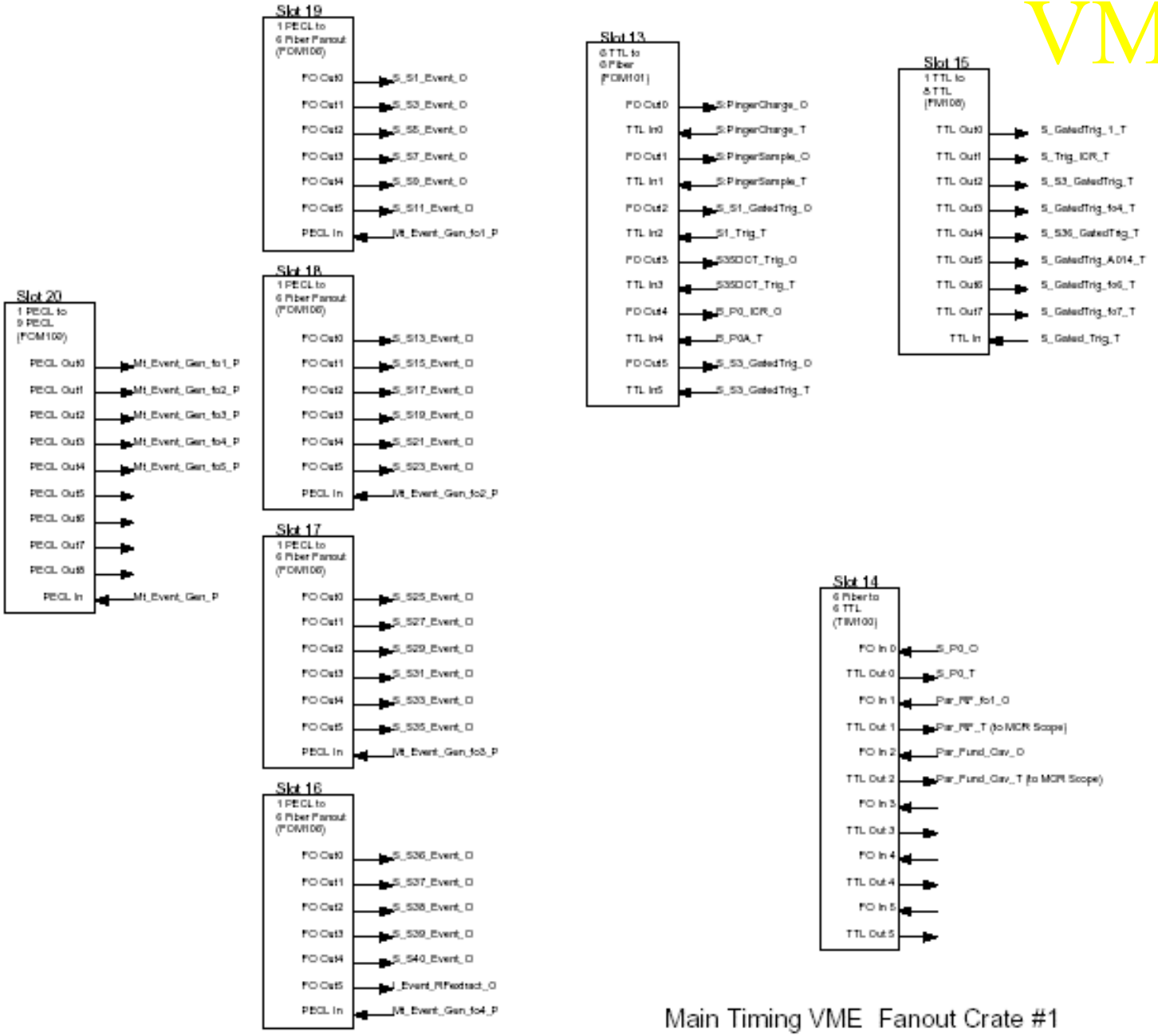
(0.5) 5 MHz
(0.25) 2.5 MHz
(0.10) 1.0 MHz
(0.05) 0.5 MHz
(0.25) 0.25 MHz
(.01) 0.1 MHz
100kHz_T
Slot 12
Fault Detector
DET100
In0
In1
In2
In3
In4
In5
In6
In7
Running
Running
Slot 7
Event Generator
Slot 8
Event Generator
Slot 9
Event Receiver
Slot 17
DDPG02
Slot 16
P0 #1 Counter
CNT100
Slot 13
P0 #2 Counter
CNT100
Slot 11
Video Sync Generator
VID100
Slot 14
BPM Timing Encoder (BTE100)
Notes:
Main Timing IOC (VME Crate #2)

VME 1



Main Timing VME Fanout Crate #1
2 of 2

F. Lenkszus/ Laird
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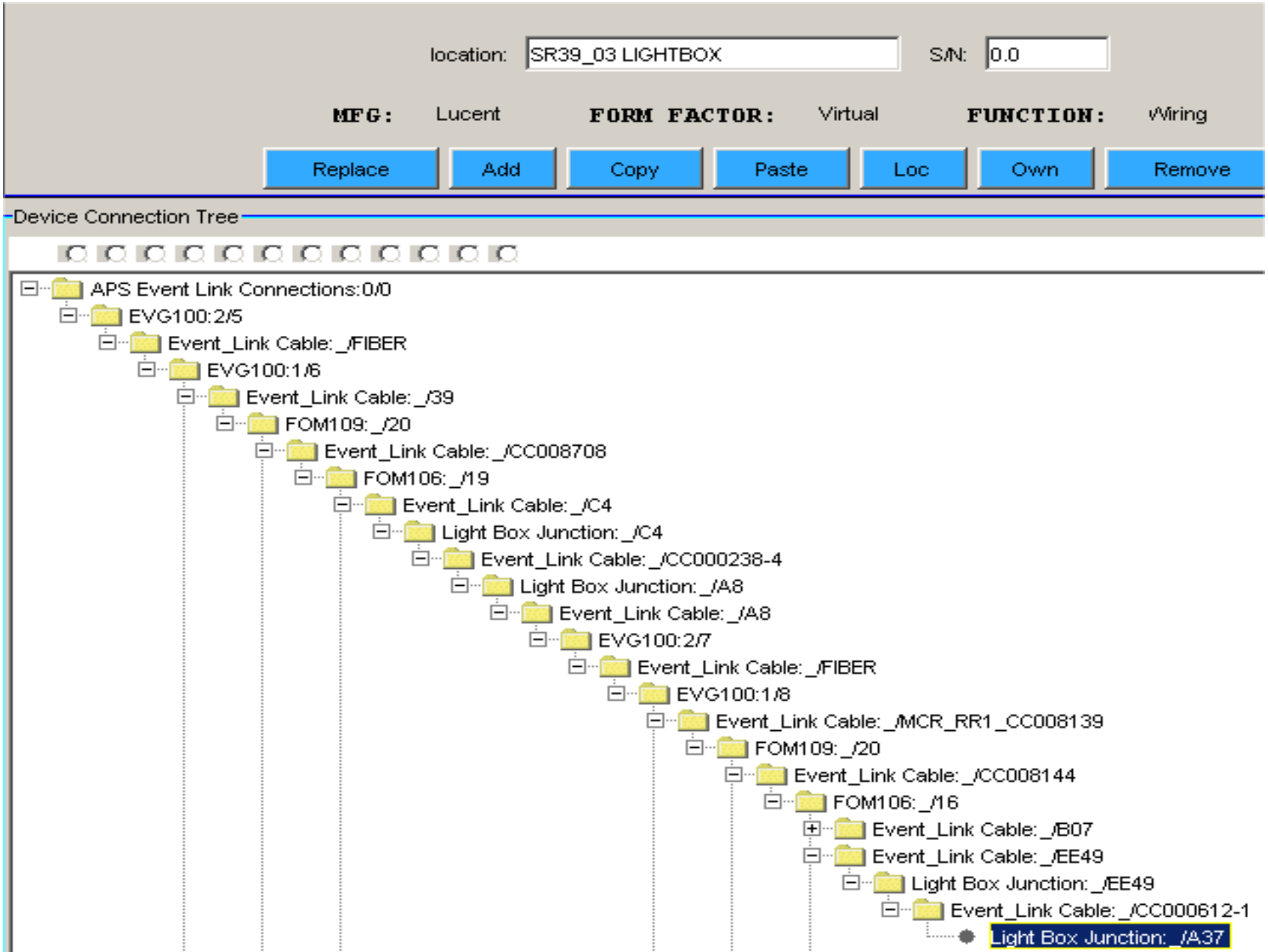
11/22/05
rev 5/9/01

CVCCT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APS Event Link Connections:0/0
EVG100:2/5
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EVG100:1/6
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FOM109: _/20
Event_Link Cable: _/CC008708
FOM106: _/19
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FOM106: _/16
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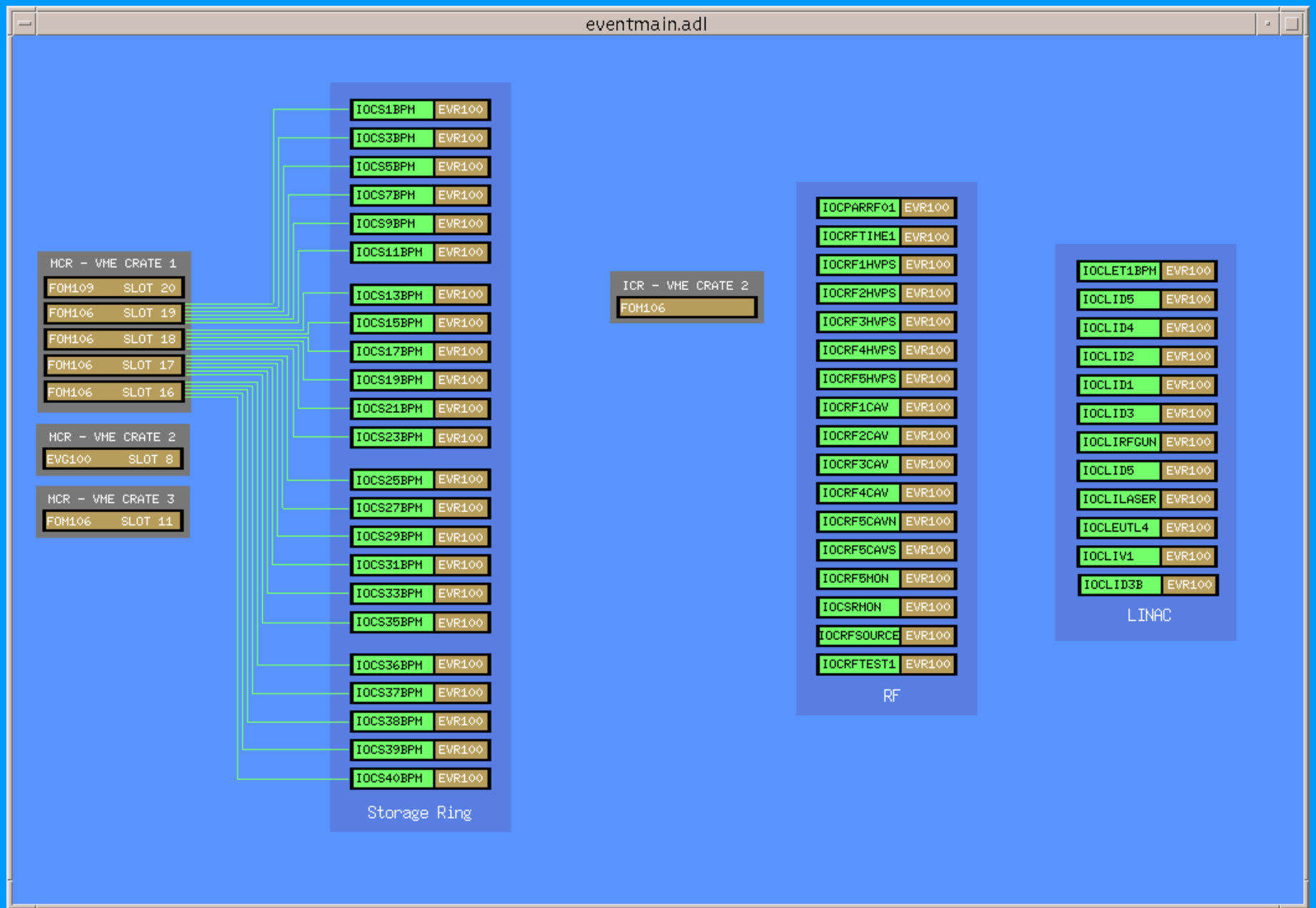
Light Box Junction: _/A37

Coming Soon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EVG100 SLOT 8
MCR - VME CRATE 3
FOM106 SLOT 11
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IOCS3BPM EVR100
IOCS5BPM EVR100
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Storage Ring
ICR - VME CRATE 2
FOM106
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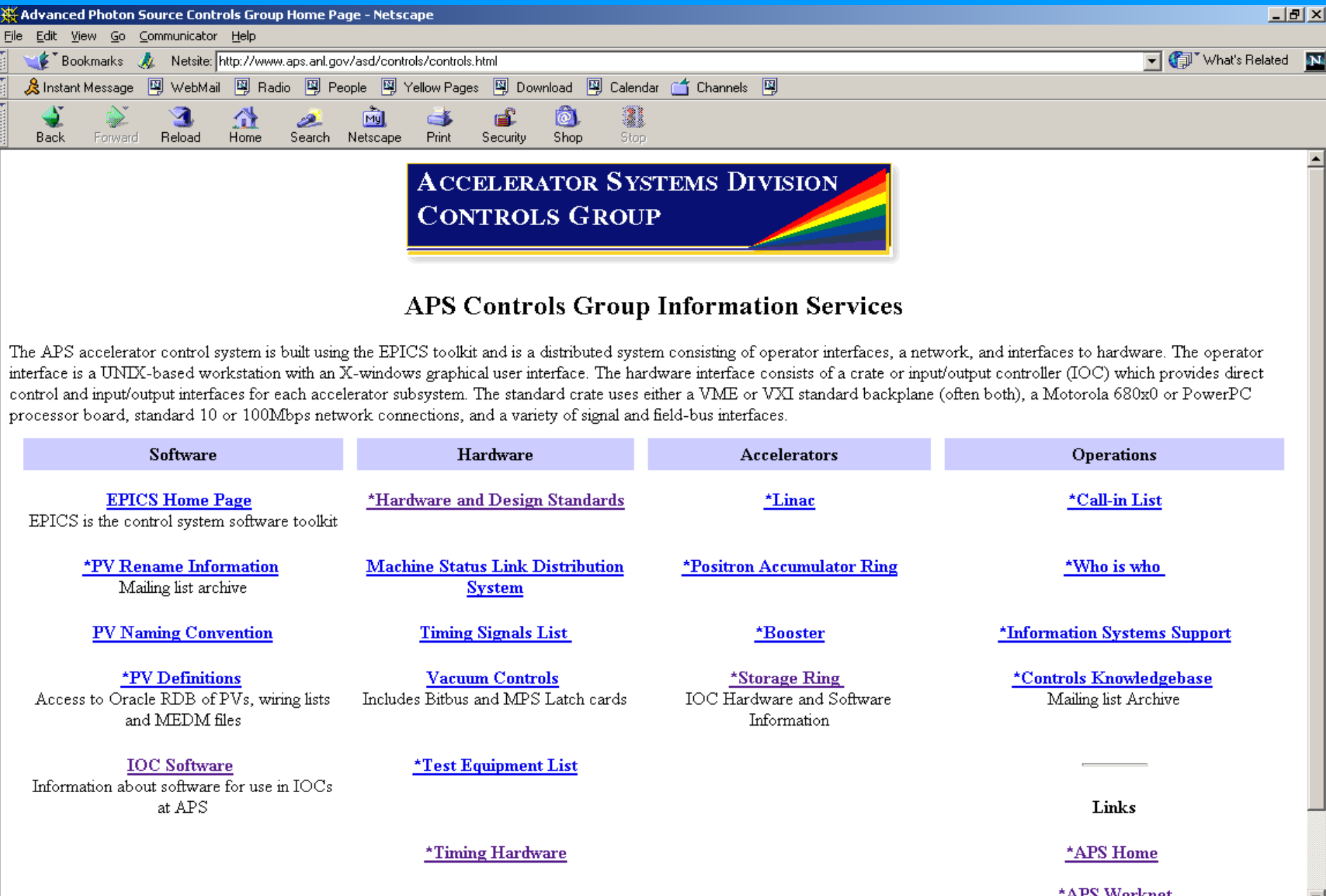
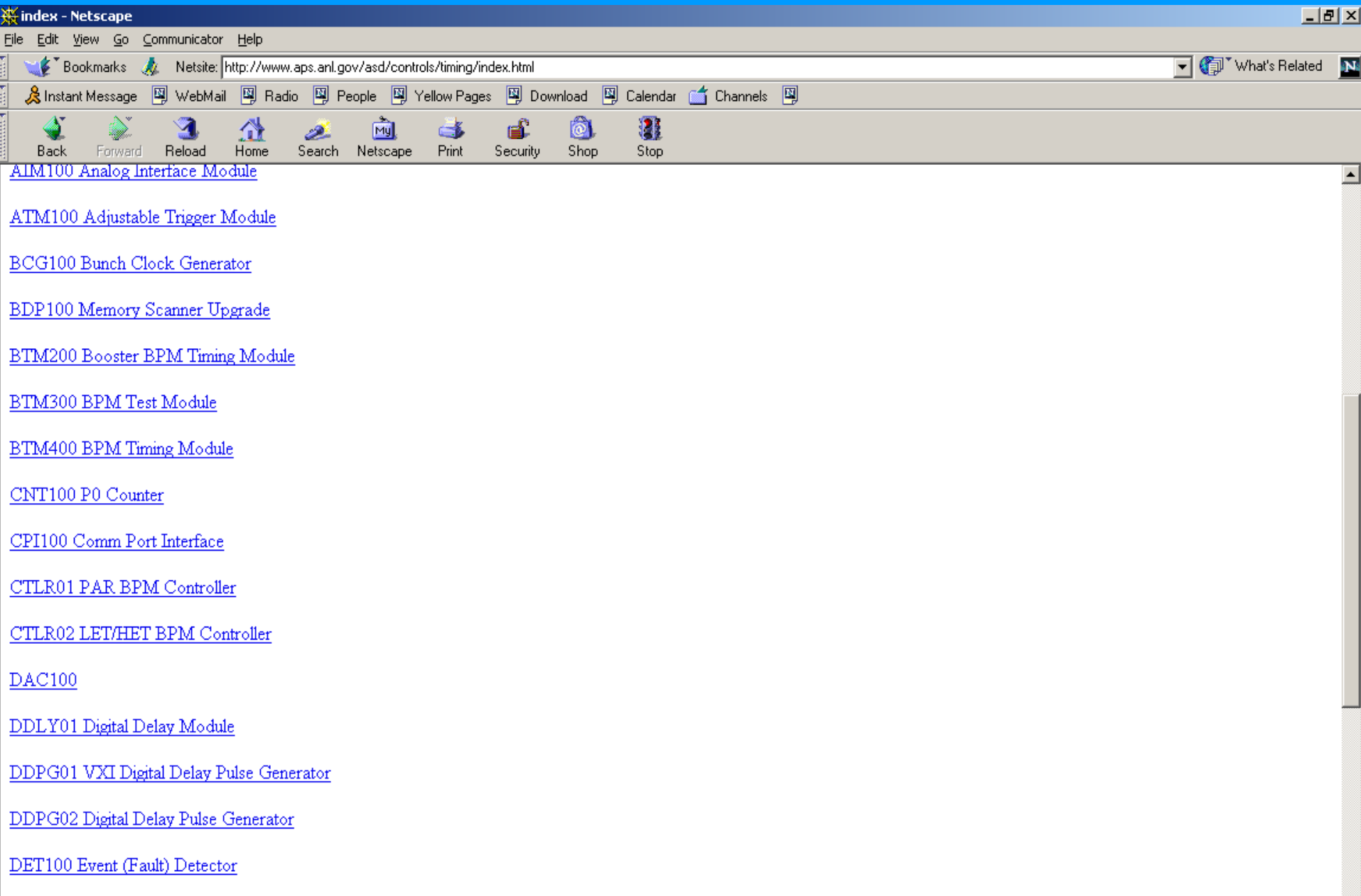
LINAC

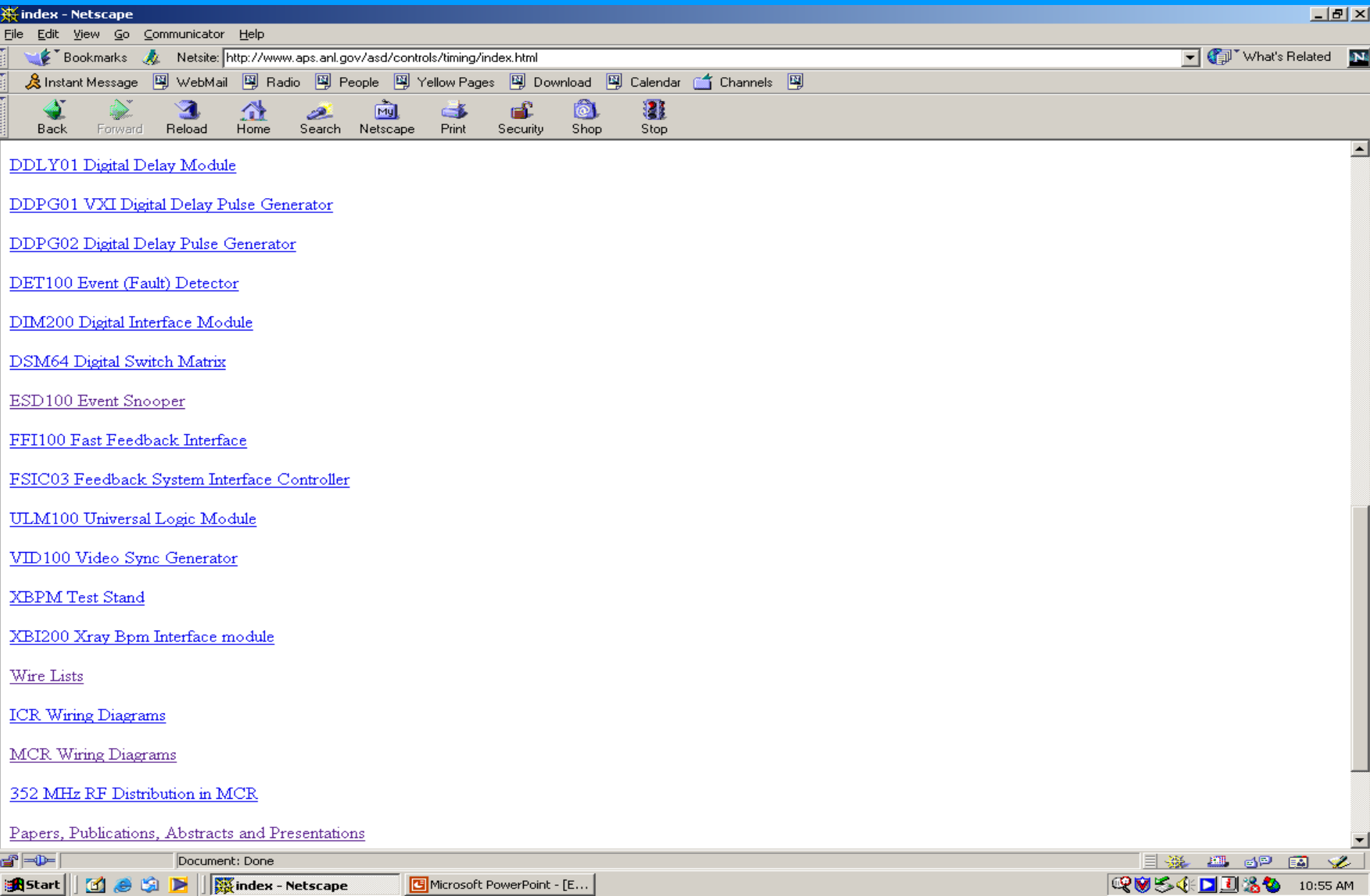
Controls Web Page



Web Index


index - Netscape
File Edit View Go Communicator Help
Bookmarks Netsite: http://www.aps.anl.gov/asd/controls/timing/index.html
What's Related
Instant Message WebMail Radio People Yellow Pages Download Calendar Channels
Back Forward Reload Home Search Netscape Print Security Shop Stop
AIM100 Analog Interface Module
ATM100 Adjustable Trigger Module
BCG100 Bunch Clock Generator
BDP100 Memory Scanner Upgrade
BTM200 Booster BPM Timing Module
BTM300 BPM Test Module
BTM400 BPM Timing Module
CNT100 P0 Counter
CPI100 Comm Port Interface
CTLR01 PAR BPM Controller
CTLR02 LET/HET BPM Controller
DAC100
DDLY01 Digital Delay Module
DDPG01 VXI Digital Delay Pulse Generator
DDPG02 Digital Delay Pulse Generator
DET100 Event (Fault) Detector

Web Index _more



Documentation

- /asdctls/documentation/components/esd100
- /asdctls/documentation/online_systems/timing/event_link_cabling.pdf
- http://www.aps.anl.gov/asd/controls/timing
  - ESD100
  - Wiring Lists
    - MCR
    - ICR
  - EVG100, EVR100, EGI100, ERI100 Coming Soon